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Reconfigurable Low-Pass Filter for Analog Baseband of Bluetooth Low Energy and Biomedical Applications

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ABSTRACT

In this study, we proposed a low-pass filter that dissipated very low power with dynamic threshold metal–oxide–semiconductor technique for Bluetooth low energy and biomedical applications of new portable Internet-of-Things devices. The operating frequency of the designed low-pass filter is between 750 and 1 MHz to meet the baseband requirements of Bluetooth and filter biomedical signals. The circuit uses two supplies to develop the performance of the circuit. The core circuit of the OTA-C filter operates on the sub-threshold region with ±0.2-V supply voltage, whereas the supply voltage of the biasing circuit is 0.6 V. The power consumption of the designed filter is 0.34 nW at 750 Hz and 376 nW at 1 MHz. The performance of the designed circuit is tested in Cadence environment with TSMC 0.18-µm technology.
Keywords: Biomedical applications, Operational Transconductance Amplifier (OTA), bluetooth low energy

Introduction

Multi-standard transceiver, which provides different standards in a single chip, should take into consideration various aspects in parallel and separate device-based solutions. Particularly, hardware sharing must be maximum between transceivers that support different standards to minimize both silicon area and static power consumption [1–5]. Some applications of Internet-of-Things (IoT) devices must provide the standards from biomedical acquisition systems to multi-standard wireless receivers [6–8]. However, even for a single application, such as Bluetooth, some circuit designs need to be reconfigurable. For example, the cut-off frequency of the analog baseband should be programmable to 1, 2.2, and 11 MHz for Bluetooth, UMTS, and WLAN, respectively [4, 9]. Biomedical applications should also operate from <1 to 10 kHz [10].

Bluetooth technologies have been developed rapidly around the world since the release of Bluetooth 2.1+EDR in 2007. Since then, Bluetooth has been used in wireless high-quality music equipment, smartphone technologies, human-interface devices, and car convenience systems. The IEEE 802.15 Working Group of special industry group (SIG) has developed the Bluetooth, and the SIG manages Bluetooth v1.1 to v5.1 [11]. The SIG, in which they were focusing on data rate (BR/EDR) for the transfer of audio signals in the past, has united with the Wibree forum and launched Bluetooth low energy (LE) v.4.0 in 2010. SIG is also currently working hard to develop LE to meet the IoT demands, where intensive work is underway. For small and low-power devices in the IoT market, LE is the best solution. Bluetooth technology is also used in health care, proximity detection, indoor positioning systems, sports and fitness [11].

When considering the low energy obtained by methods such as energy harvesting, circuits such as filters and LNA with very low-power consumption designed for Bluetooth LE are important, in which they are used in communication required for IoT applications [12, 13].

To meet the wireless features of Bluetooth and biomedical applications, we designed a low-pass filter (LPF) with a wide range of settings based on G_m–C filter topology, which consumes very low power, suitable for Bluetooth LE and biomedical signal acquisition devices used in

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IoT applications. To improve the performance of operational transconductance amplifiers (OTA) acting as G_m block, we used the cross-coupled transistors as the output stage of the OTA structure. However, we selected the supply voltage of the biasing transistors larger than the main circuit to increase the dynamic range of the design. The supply voltages of the core design and the biasing circuit are ±0.2 and 0.6 V, respectively. To improve the performance of transistors, we implemented the designed circuit with dynamic threshold metal–oxide–semiconductor (DTMOS) technique in the sub-threshold region [14–16].

The rest of the paper is organized as follows. Section 2 gives the voltage mode G_m–C filter. Section 3 describes the CMOS realization of G_m–C filter and explains the importance of the dual supply. Section 4 illustrates the layout of the second-order Butterworth filter structure and gives the transient and AC analysis of the filter with the third-order intercept point (IIP3) and noise analysis; additionally, the performance of the designed filter is justified by comparing conventional designs. Section 5 concludes this paper.

Voltage Mode G_m–C Filter

If noise-filtering is incorporated into the biomedical signal acquisitions systems, the use of LPF and analog-to-digital conversion are indispensable. In CMOS technology, LPF designs operating in the deep sub-threshold region are preferred to minimize power consumption and silicon area and can also be used in Bluetooth LE designs [17–19].

G_m–C topologies are useful in performing analog filters. When designing filters for a multi-standard signal acquisition system, the design of reconfigurable circuits is as important as low-power consumption. For several decades, the frequencies of interest may vary depending on the nature of different applications or physical signals. Thus, it is more economical to design and manufacture reconfigurable hardware that can meet different specifications. Among the various filter architectures, G_m–C filters have become popular choices in the design of continuous-time filters because of their easy adjustment capabilities and low-power consumption [17–22].

Generally, G_m–C designs consume low power and can be designed for low-frequency applications. It is possible to design a lower-power consuming OTA with small transconductance in weak inversion so that the capacitor used takes up less area on the chip [20–22].

Figure 1 shows the structure of the implemented OTA-C filter. The transfer function of LPF is given in Equation (1) as follows:

$$\frac{V_{LP}}{V_{in}} = \frac{g_{m1}g_{m2}}{s^2C_1C_2 + sC_1g_{m2} + g_{m1}g_{m2}} \quad (1)$$

where g_m denotes the transconductance of OTA.

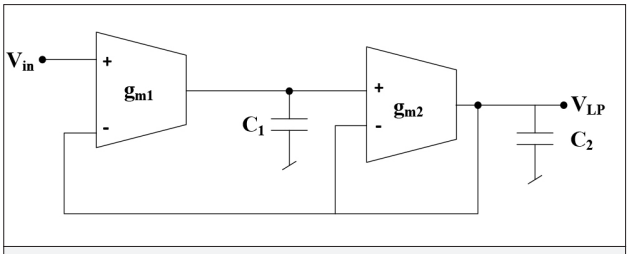

Figure 1. Voltage-mode second-order OTA-C LPF

Equations (2) and (3) give the resonance frequency (ω_0) and quality factor (Q), respectively.

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (2)$$

$$Q = \sqrt{\frac{C_2g_{m1}}{C_1g_{m2}}} \quad (3)$$

3. CMOS Implementation of the Designed Filter

Figure 2 shows the CMOS implementation of LPF designed for analog baseband of Bluetooth LE and biomedical signal acquisition systems. The design of the proposed filter is implemented with 0.18-µm TSMC technology using DTMOS technique. The transistor aspect ratio of transistors in core design is 0.36 µm/0.36 µm, and the aspect ratio of the biasing transistors is 10 µm/2 µm. and are 10 kΩ, and C_1 and C_2 are 50fF.

In improving the performance of the MOS transistors with the same power dissipation, previous studies have investigated different techniques such as DTMOS [15, 23–25]. DTMOS shows high-current gain under the same supply voltage of standard CMOS transistor. The low-threshold characteristic of DTMOS increases the gain of transistors. In terms of power dissipation with the same gain, DTMOS is more useful in the design of analog circuits [26]. The realization of DTMOS is based on connecting the device gate and body, which changes dramatically the threshold voltage of the transistor using the relationship given in Equation (4). DTMOS has a higher transconductance than the standard CMOS transistor under the same V_{GS} voltage. The threshold voltage with $V_{BS} = 0$ is denoted by V_{th0}. γ and φ_F are technology-dependent parameters having typical values of $0.4/\sqrt{V}$ and 0.4V, respectively. Equation (5) gives the transconductance under the sub-threshold region.

$$|V_{th,p}| = |V_{th0,p}| + \gamma_p(\sqrt{|2\Phi_F| + V_{BS}} - \sqrt{|2\Phi_F|}) \quad (4)$$

$$g_m = \frac{I_D}{nV_T} \quad (5)$$

In Figure 2, only the pMOS transistors are implemented by DTMOS transistors because of the restriction of the double-well structure of the used 0.18-µm technology. The expensive triple well (deep *n*-well) technology is appropriate in designing both nMOS and pMOS transistors with DTMOS technique. Here, we used double-well technology to design the proposed filter because it is cheap.

The conventional symmetrical OTA is modified with M_1, M_6, M_9, and M_{12} transistors to operate at ±0.2 V. Figure 3(a) shows the conventional symmetrical OTA. C_c (100 fF) is the compensation capacitance. The voltage gain of the conventional symmetrical OTA denoted by A_{V1} is represented in Equation (6), whereas A_{V2} of the proposed circuit given in Figure 3(b) is changed to Equation (7).

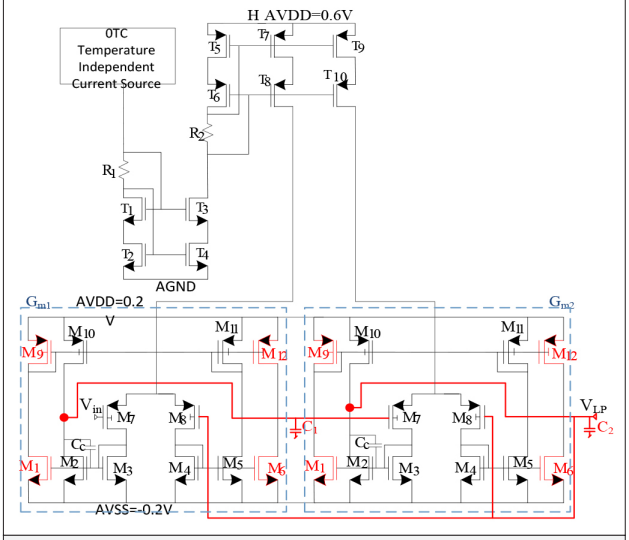

Figure 2. The CMOS implementation of the voltage-mode LPF

$$A_{V1} \cong \frac{V_o}{V_{in}} = \frac{g_{m7,8}}{g_{m3.4}} \frac{g_{m2,10}}{g_{ds2.10}} \tag{6}$$

$$A_{V2} \cong \frac{V_o}{V_{in}} = \frac{g_{m7,8}}{g_{m3.4}} \frac{g_{m2,10}}{g_{m9}} \tag{7}$$

$g_{m3,4}$ and $g_{m7,8}$ are constant. $\Delta g_{m3,4}=0$ and $\Delta g_{m7,8}=0$ because the current flowing through M_3, M_4, M_7, and M_8 are constant. Thus, Equation (7) with the change in g_m represented as Δg_m can be rewritten in the following Equation (8).

$$A_{V2} \cong \frac{V_o}{V_{in}} = \frac{g_{m7,8}}{g_{m3,4}} \frac{(g_{m2,10} + \Delta g_{m2,10})}{(g_{m9} + \Delta g_{m9})} \tag{8}$$

In the design, transistors are biased in the sub-threshold region. Thus, the change in their transconductance, , and can be expressed in the following Equation (9).

$$\Delta g_{m2,10} = \frac{2\Delta I_{DS2,10}}{nV_T}, \Delta g_{m9} = \frac{2\Delta I_{DS9}}{nV_T} \tag{9}$$

I_{DS9} is equal to $I_{DS3,4}$ in the condition of the same ratio of M_3–M_2 and M_4–M_5. Substituting Equation (9) into Equation (8) leads to Equation (10) [27].

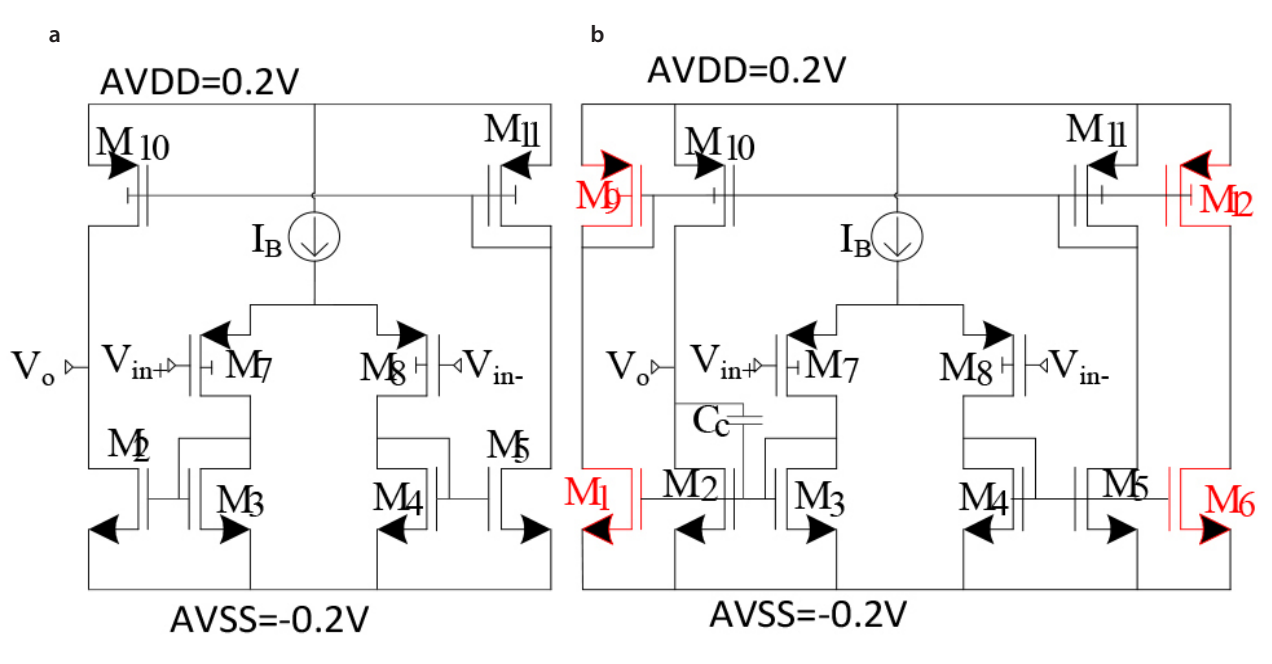

Figure 3. a, b. (a) The conventional symmetrical OTA and (b) the recommended circuit

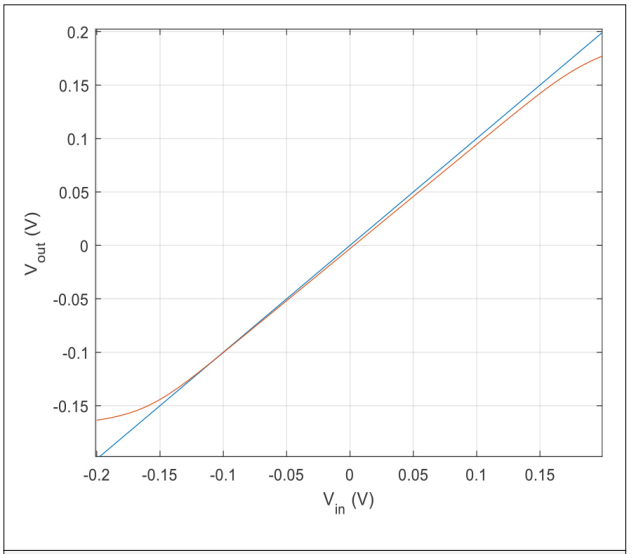

Figure 4. The dc sweep of the designed CMOS OTA between –0.2 and +0.2 V with unity feedback

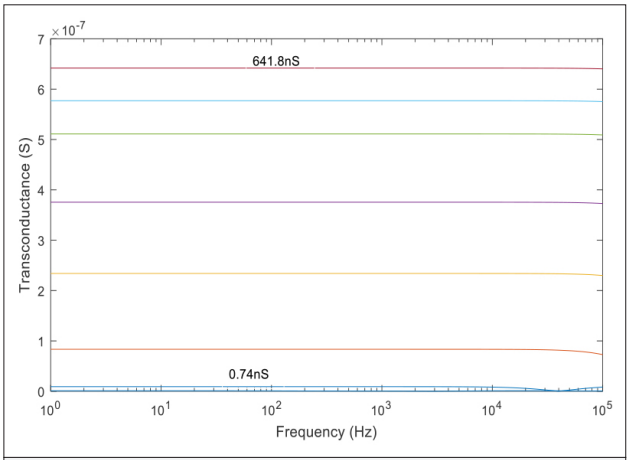

Figure 5. The transconductance of the designed OTA according to the biasing currents

$$A_{V2} \cong \frac{V_o}{V_{in}} = \frac{g_{m7,8}}{g_{m3,4}} \frac{(g_{m2,10} + \frac{2\Delta I_{DS2,10}}{nV_T})}{(g_{m9} + \frac{2\Delta I_{DS9}}{nV_T})} \quad (10)$$

Figure 4 shows the dc sweep of the designed CMOS OTA between –0.2 and +0.2 V. Figure 5 shows the simulated transconductance of the designed OTA according to the biasing current. The transconductance of the proposed circuit is given in Equation (11). Table 1 shows the values of transconductance according to the biasing current.

$$\frac{I_o}{V_{in}} = \frac{g_{m7,8}}{g_{m3.4}} (g_{m2,10} + \frac{2\Delta I_{DS2,10}}{nV_T}) \quad (11)$$

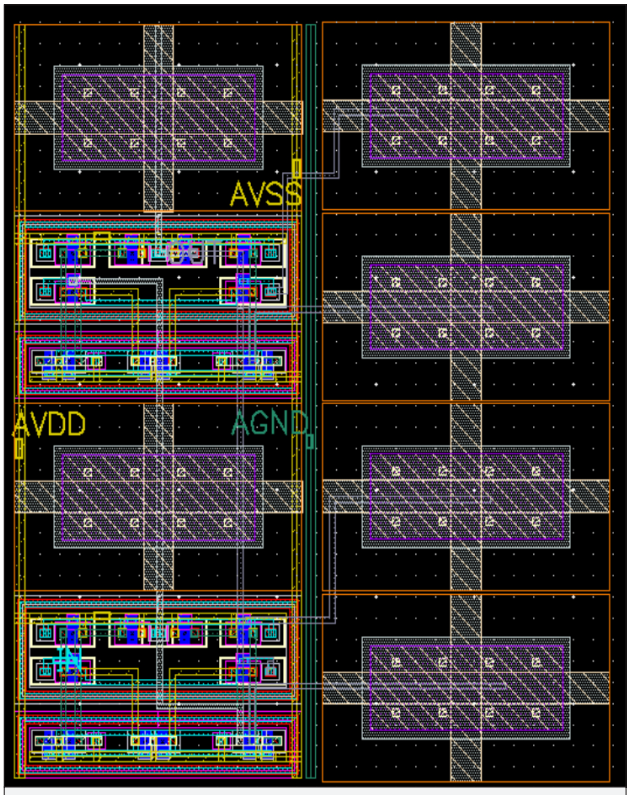

Figure 6. The layout of the designed filter (30.2 µm×35.45 µm; 0.00107 mm²)

Table 1. Biasing current versus transconductance

Biasing current (nA)	Transconductance (nS)
0.1	0.74
1	9.3
10	83.2
30	233.9
50	375.4
70	511
80	576
90	641.8

By adding M_1, M_6, M_9, and M_{12} transistors, we reduced G_m of OTA to support biomedical applications with Bluetooth LE in the same design. In the g_m reduction method, the second stage gain is minimized by decreasing the output high impedance. The simulated G_m in conventional design is obtained as 1.07 nS with 0.1 nA biasing current, whereas G_m of the proposed design is 0.745 nS with 0.1 nA.

We used two different supply voltages to improve the design's dynamic range. For example, T_8 and T_{10} transistors cause the

Table 2. Improvement in basic OTA performance quantities provided by different H_AVDD values

H_AVDD	THD	Power	Noise @ 10 kHz	*f* (-3dB)	Gm
0.4V	9.41%	109 nW	1.01 µV/√Hz	276 kHz	213.2 nS
0.6V	4.96%	115 nW	1 µV/√Hz	304 kHz	233.9 nS

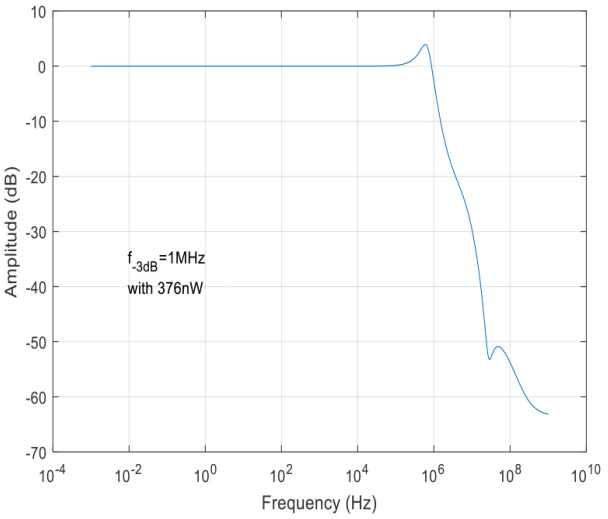

Figure 7. The simulation of the second-order LPF (f_(-3dB)=1 MHz for 376-nA biasing current of both OTA)

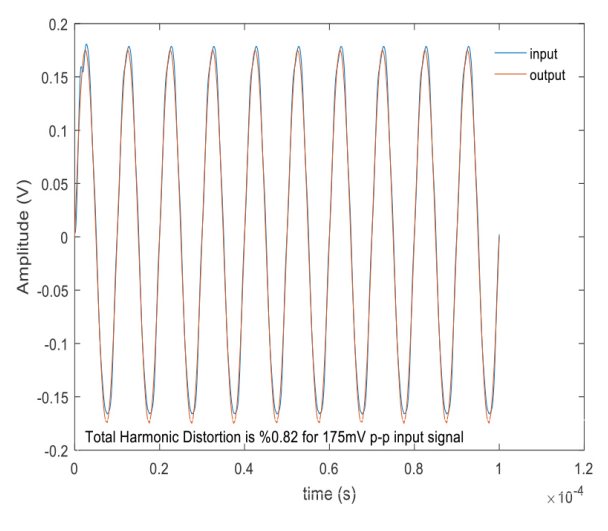

Figure 8. The transient response of the designed filter for 175-mV peak-to-peak input signal at 10 kHz

voltage to decrease to 2 V_{ON} at the output, assuming that they operate in the saturation region. V_{ON} denotes the minimum voltage of saturation as $V_{ON} = V_{GS} - V_{TH}$.

2 V_{ON} is not important because MOSFET is performed in the sub-threshold region; however, a larger value must be used

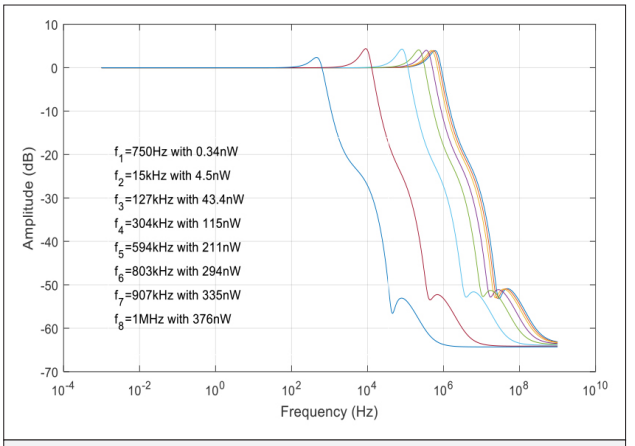

Figure 9. The AC response of the designed filter for different cut-off frequencies

for the supply voltage of the biasing transistors to improve the dynamic range. Although MOSFET behaves like BJT in the sub-threshold region, the drain current is still depended [26] to the $(V_{GS} - V_{th})$, as given in Equation (12).

$$I_D = C_{OX}.\mu_{eff}\frac{W}{L}.n.V_T^2.e^{(v_{GS}-v_{th})/nV_T} \quad (12)$$

In the design, the headroom is enlarged by transistors operating in the sub-threshold region and using two different supply voltages. The voltage drop is approximately simulated as 0.05 V given in Figure 4 for 0.6-V supply voltage of biasing transistors.

4. Layout and its Simulations

Figure 6 shows the layout of the designed circuit. The core occupation areas of the designed circuit are 30.2 µm × 35.45 µm and 0.00107 mm². Figure 7 shows the post-layout simulation of the second-order LPF. The cut-off frequency of the designed filter is 1 MHz for the 90-nA biasing current of both OTAs.

Figure 8 shows the transient response for 175-mV peak-to-peak input signal at 10-kHz frequency. The total harmonic distortion is 0.82%. The boundary for the input level of the design is 175 mV. The designed filter has low distortion for the low-input level. The big value selection of the biasing circuit's supply improves the input common-mode range of the designed filter.

The cut-off frequency of the designed filter can be programmable with the biasing current, as shown in Figure 9. The maximum power dissipation of the designed circuit is 376 nW at 1-MHz cut-off

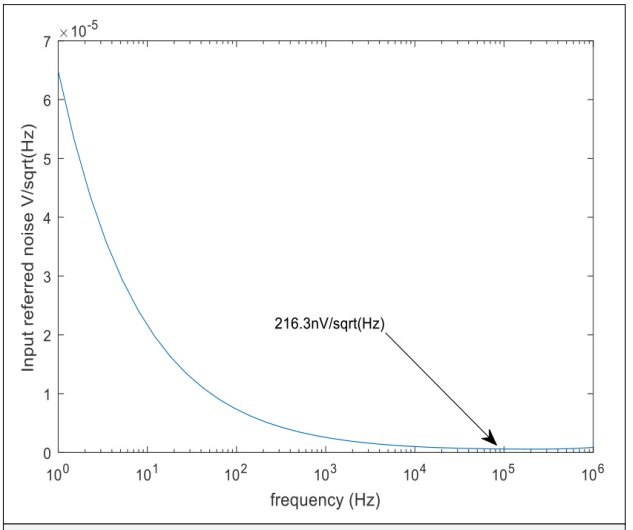

Figure 10. The input-referred noise of the proposed filter

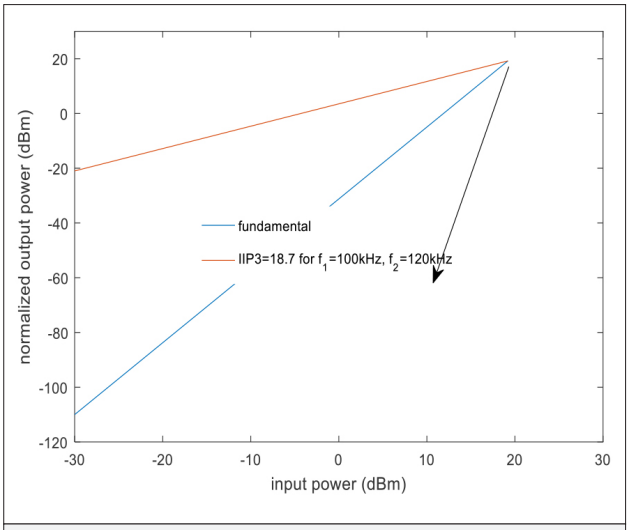

Figure 11. Third-order intercept point (IIP3)

Table 3. Comparison of the designed filter with state of the art

Specification	[9]	[29]	[30]	[31]	[13]	[7]	This work
Technique	*Gm–C*	Active RC	Active RC	Active RC+DT	Active RC	*Gm–C*	*Gm–C*
Technology (µm)	0.18	0.12	0.13	0.065	0.18	0.090	0.18
Order	3	5	5	4	4	4	2
Bandwidth (MHz)	0.5	5	19.7	10	0.6	12	1
DC gain (dB)	0	0	2	0	10	0	0
Input noise	425	140	30	22.8	126	293.6	216.3
IIP3 (dBm)	22.3	20	18.3	11	25	28	18.7
SFDR (dB)	57.3	73	69	58	65.6	NA	NA
Power @ VDD	4.1 m @ 1.2 V	6.1 m @ 1 V	11.25 m @ 1.5 V	10.8 m @ 1.8 V	0.5 m @ 1.8 V	11.83 m @ 1.2 V	0.34 nW @ 0.4–0.6 V
Chip area (mm^2)	0.23	0.25	0.2	0.75	0.14	NA	0.00107
FoM ($\frac{W \times mm^2}{dBm \times H}$)	28.1p	3.05p	1.24p	3.92p	33.3p	NA	1.28f

frequency, whereas the minimum power dissipation is 0.34 nW. The operation of the designed filter is appropriate to Bluetooth applications and biomedical applications because of the need for low-power design of biomedical circuits and Bluetooth LE.

Table 2 shows the performance comparison of dual supply design for two different H_AVDD values at 30-nA biasing current of I_B. The implementation of a double supply decreases the total harmonic distortion of the designed filter. Furthermore, the cut-off frequency and G_m of the designed filter are increased by the proposed technique. By increasing the supply of the biasing circuit from 0.4V to 0.6V, we increased the G_m of OTAs for 30-nA tail current from 213.2 to 233.9 nS, thus increasing the cut-off frequency of the designed circuit from 276 to 304 kHz. Although the proposed method improved circuit performance by 15%–20%, power consumption increased by only 5%. It may seem like a disadvantage to obtain two different supply voltages in the circuit. However, AVDD can be easily achieved using asymmetrical supply.

Input referred noise of the designed filter is 216.3 nV/sqrt(Hz), as shown in Figure 10.

The IIP3 of the proposed filter is 18.7 dBm, as shown in Figure 11. IIP3 is tested for the 100 and 120 kHz tones. The required IIP3 value for the application of Bluetooth is 17.3 dBm [28].

Table 3 gives the comparison of the proposed circuit with conventional studies. The design is considered to be very successful when compared with the defined figure of merit (FoM) given in Equation (13). It has a very good performance compared with the recommended circuit, especially in terms of power consumption and core occupation area on the chip.

$$FoM = \frac{power\ x\ area}{order\ x\ IIP3\ x\ bandwidth} \quad (13)$$

Conclusions

This study proposed OTA-C filter for the baseband of Bluetooth LE and biomedical signal acquisition systems with DTMOS technique. The filter is designed with OTA-C filter topology with dual supply voltage: ±0.2 V (core circuit) and +0.6 V (biasing circuit). We investigated a new implementation for the output stage of the symmetrical OTA. The input-referred noise of the designed filter is 216.3 nV/sqrt(Hz), and IIP3 of the designed filter is 18.7 dBm. In terms of FoM, the designed baseband filter is considered to be very efficient. Simulations are performed in Cadence environment with 0.18-µm TSMC technology.

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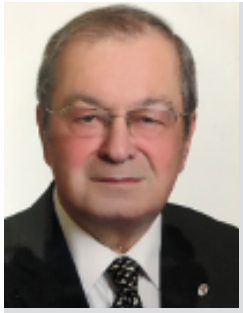

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